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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CONTINO, PAUL F	
ART UNIT	**PAPER NUMBER**
2114	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/27/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/699,305	BILLICK ET AL.	
	Examiner	Art Unit	
	Paul Contino	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,10-12,14-19,21,22 and 24-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,10-12,14-19,21,22 and 24-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION: Non-Final Rejection

Response to Arguments

1. Applicant's arguments with respect to claims 1-7, 10-12, 14-19, 21, 22, and 24-29 have been considered but are moot in view of the new grounds of rejection.

Claim Objections

2. Claim 29 is objected to because of the following informalities: line 5 states "each populated memory system memory" where the term "populated" lacks antecedent basis. The Examiner is unsure as to what the Applicant is referring with respect to the term "populated". Appropriate correction is required.

3. Claim 21 is objected to because of the following informalities: claim 21 is stated as depending from claim 20, which has been cancelled. In order to apply prior art, the Examiner is interpreting claim 21 in the broadest reasonable means as being dependent from claim 15. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 10-12, 14-18, and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Award BIOS (*ASUS TR-DLS Dual Socket 370 Motherboard User's Manual*).

As in claim 10, Award BIOS discloses software for managing a memory system having a plurality of memory system devices, the software embodied in computer readable media and when executed operable to:

receive a user selection of an operating state for a selected memory system device *(Page 67, enabling/disabling of DIMMs via BIOS interface)*;

alter the operating state of the selected memory system device in accordance with the user's operating state selection *(Page 67, enabling/disabling of DIMMs)*; and

disable the selected memory system device *(Page 67, disabling of DIMMs)*.

As in claim 11, Award BIOS discloses communicating an operating state for each memory system device *(Page 67, where each DIMM and DIMM state is alterable)*.

As in claim 12, Award BIOS discloses maintaining the selected operating state through subsequent information handling system boot operations *(Page 67, where the purpose of enabling/disabling [altering state] is for future process affects)*.

As in claim 14, Award BIOS discloses disabling a memory card slot of the memory system, the memory card slot adapted to support a dual-channel memory card *(Page 67, where a DIMM is a memory card slot that supports a dual-channel memory card)*.

As in claim 15, Award BIOS discloses an information handling system, comprising:

a plurality of memory slots operable in at least one of a plurality of operating states *(Page 67, DIMM slots in an enabled/disabled state)*;

at least one processor operably coupled to the memory slots *(Page 67, inherent that a processor is coupled to memory slots)*; and

a program of instructions embodied in computer readable media and executable by the processor *(Page 67 BIOS)*, the program of instructions operable to:

effect a user selected operating state for at least one of the plurality of memory slots *(Page 67, the user is able to select the state of enabled/disabled for a DIMM memory slot)*; and

allow a user to selectively toggle the operating state for each of the plurality of memory slots between enabled and disabled *(Page 67, enabled/disabled per DIMM)*.

As in claim 16, Award BIOS discloses displaying a memory slot representation corresponding to a respective one of the plurality of memory slots *(Page 67, where the BIOS tabular display of DIMMs is a memory slot representation)*; and

communicate an operating status for each displayed memory slot representation, the operating status corresponding to an operating state for each respective memory slot *(Page 67,*

where the displaying of the disabled/enabled state is communication of respective operating statuses).

As in claim 17, Award BIOS discloses a basic input/output system memory operably coupled to the processor *(Page 67, inherent in order to store the BIOS [Award BIOS])*;

a basic input/output system program stored in the basic input/output system memory *(Page 67, the BIOS itself)*; and

the program of instructions incorporated in the basic input/output system program *(Page 67, inherent to Award BIOS).*

As in claim 18, Award BIOS discloses the program of instructions operable to maintain the selected operating state of the memory devices through additional information handling system operations *(Page 67, where the purpose of enabling/disabling [altering state] is for future process affects).*

As in claim 21, Award BIOS discloses preventing communication with a memory module disposed in a memory slot in the disabled operating state *(Page 67, purpose of disabling a DIMM).*

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-4, 7, 19, 22, and 25-28 are rejected under 35 U.S.C. 103(a) as being obvious over Award BIOS in view of Stern et al. (U.S. Patent No. 7,000,159).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

As in claim 1, Award BIOS teaches software for diagnosing a memory system including a plurality of memory system devices *(Page 67, BIOS)*, the software embodied in computer readable media and when executed operable to:

provide an interface for user selection of at least one memory system device for isolation *(Page 67, the screen interface with DIMM disable/enable selection allowing isolation)*; and

facilitate isolation of the at least one selected memory system device by disabling all system memory devices except the at least one selected memory device or disabling the at least one selected memory device *(Page 67, where disabling all but one DIMM allows for isolation of a memory device)*.

However, Award BIOS fails to explicitly teach of performing diagnostics on the isolated device. Stern et al. teaches of performing diagnostics on a memory device *(column 3 lines 38-44, 52-53, column 5 lines 49-51, and column 6 lines 8-17, where diagnostics of a DIMM occur during the POST of BIOS)*.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the diagnostics as taught by Stern et al. in the invention of Award BIOS. This would have been obvious because a power-on self test (POST), where system memory diagnostics occur, is a standard and well-known operation integrated with system BIOS. After configuring the memory of a BIOS, such as is disclosed in Award BIOS, diagnostics such as those taught by Stern et al. will occur on the enabled DIMM memory modules.

As in claim 2, Award BIOS teaches repeating the facilitate and perform operations for each memory system device *(Page 67; where a user may disable/enable any DIMM and a POST will run diagnostics on that memory device)*.

As in claim 3, Stern et al. teaches of logging one or more results from the memory system device diagnostic test *(column 4 lines 27-28, recording)*.

As in claim 4, Award BIOS teaches maintaining isolation of each memory system device whose diagnostic test indicates faulty operation *(Page 67, where the DIMM will remain isolated if there is indication of a fault. The only time a DIMM will come out of isolation is if a user edits the BIOS).*

As in claim 7, Award BIOS teaches effecting the facilitate and perform operations on at least one memory slot of the memory system *(Page 67, where if more than one DIMM is enabled, the facilitate and perform operations will be).*

As in claim 19, Award BIOS teaches of a program of instructions. However, Award BIOS fails to teach of diagnostics. Stern et al. teaches of initiating a diagnostic routine, the diagnostic routine operable to test at least one enabled memory slot *(column 4 lines 5-13).*

It would have been obvious to a person skilled in the art at the time the invention was made to have included the diagnostics as taught by Stern et al. in the invention of Award BIOS. This would have been obvious because a power-on self test (POST), where system memory diagnostics occur, is a standard and well-known operation integrated with system BIOS. After configuring the memory of a BIOS, such as is disclosed in Award BIOS, diagnostics such as those taught by Stern et al. will occur on the enabled DIMM memory modules.

As in claim 22, Award BIOS teaches a method for identifying faulty devices in a memory system including a plurality of memory slots and a plurality of memory modules disposed in at

least a portion of the plurality of memory slots and wherein the memory slots are controllable from a basic input/output system (BIOS) utility *(Page 67)*, comprising:

receiving from a user selection of a memory system device for isolation *(Page 67, disabling of DIMMs)*;

isolating, via a BIOS utility setting, the memory system device selected by the user *(Page 67, if all but one DIMM is set to disabled)*; and

disabling any remaining memory system devices via the BIOS utility setting *(Page 67, disabling of any Side of the remaining DIMM; Page 52, Ultra DMA Mode disabling)*.

However, Award BIOS fails to explicitly teach of performing diagnostics on the isolated device. Stern et al. teaches of performing diagnostics on a memory device operable to produce at least one result *(column 3 lines 38-44, 52-53, column 4 lines 5-13, column 5 lines 49-51, and column 6 lines 8-17, where diagnostics of a DIMM occur during the POST of BIOS; column 4 lines 27-29 teach a result of diagnostics as a record of the test)*.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the diagnostics as taught by Stern et al. in the invention of Award BIOS. This would have been obvious because a power-on self test (POST), where system memory diagnostics occur, is a standard and well-known operation integrated with system BIOS. After configuring the memory of a BIOS, such as is disclosed in Award BIOS, diagnostics such as those taught by Stern et al. will occur on the enabled DIMM memory modules.

As in claim 25, Stern et al. teaches of performing diagnostic testing on a memory module associated with the isolated memory system device *(column 3 lines 38-44, 52-53, column 5 lines*

49-51, and column 6 lines 8-17, where the memory isolated [enabled] by Award BIOS is the only memory being tested).

As in claim 26, Stern et al. teaches of performing diagnostic testing on a memory module associated with the isolated memory system device *(column 3 lines 38-44, 52-53, column 4 lines 5-13, column 5 lines 49-51, and column 6 lines 8-17, where the memory slot associated with the memory device isolated [enabled] by Award BIOS is the only memory slot being tested).*

As in claim 27, Stern et al. teaches of reporting any memory system devices whose diagnostic test results indicated faulty operation *(column 4 lines 10-13, where a pattern mismatch indicates a fault).*

As in claim 28, Award BIOS teaches of maintaining, via BIOS utility settings, disability of those memory system devices whose diagnostic test results indicate faulty operation *(Page 67, where the DIMM will remain disabled if there is indication of a fault. The only time a DIMM will come out of isolation is if a user edits the BIOS).*

* * *

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being obvious over Award BIOS in view of Stern et al., further in view of POST (*AWARDBIOS 6.0 User Guide*).

As in claim 5, the combined invention of Award BIOS and Stern et al. teaches of memory system devices. However, the combined invention of Award BIOS and Stern et al. fails to teach of reporting each memory device whose diagnostic test indicates faulty operation. POST teaches of reporting each memory device whose diagnostic test indicates faulty operation *(pages 48-54, where there are POST error messages for each memory device that fails)*.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the fault reporting as taught by POST in the combined invention of Award BIOS and Stern et al. This would have been obvious because the BIOS used for memory selection in POST is the same BIOS (Award BIOS™) as in Award BIOS.

* * *

7. Claims 6 and 24 are rejected under 35 U.S.C. 103(a) as being obvious over Award BIOS in view of Stern et al., further in view of Bakke et al. (U.S. Patent No. 6,971,049).

As in claims 6 and 24, the combined invention of Award BIOS and Stern et al. teaches memory device isolation. However, the combined invention of Award BIOS and Stern et al. fails to teach of repeating the facilitate and perform operation for each device. Bakke et al. teaches of repeating isolation and diagnostics for each memory device in a plurality of memory devices *(column 2 lines 28-35, column 5 lines 30-42, and column 6 lines 33-64)*.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the repeating as taught by Bakke et al. in the combined invention of Award BIOS and Stern et al. This would have been obvious because a single device can be

pinpointed in order to determine why a system is failing. Further, the isolation and diagnostics taught by Bekke et al. may occur during a boot sequence *(column 7 lines 36-44)* such as that taught by Award BIOS and Stern et al.

* * *

8. Claim 29 is rejected under 35 U.S.C. 103(a) as being obvious over Award BIOS in view of Stern et al., further in view of POST, further in view of Bassman et al. (U.S. Patent No. 6,408,334).

As in claim 29, the combined invention of Award BIOS and Stern et al. teaches of diagnostic tests on an isolated memory device. However, the combined invention of Award BIOS and Stern et al. fails to teach of logging results of tests and reporting results to a user. Bassman et al. teaches of logging diagnostic tests *(column 4 lines 29-35)*. POST teaches of reporting diagnostic results to a user *(pages 48-54)*.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the logging of results as taught by Bassman et al. in the combined invention of Award BIOS and Stern et al. This would have been obvious because keeping a record of results allows for a means of discovering exactly what a fault was that occurred in order to remedy such a fault.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the fault reporting as taught by POST in the combined invention of

Award BIOS, Stern et al., and Bassman et al. This would have been obvious because the BIOS used for memory selection in POST is the same BIOS (Award BIOS™) as in Award BIOS.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Contino whose telephone number is (571) 272-3657. The examiner can normally be reached on Monday-Friday 9:00 am - 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SCOTT BADERMAN
SUPERVISORY PATENT EXAMINER

PFC
3/16/2007